

### 9N90H-VB TO247 Datasheet

### N-Channel 900V (D-S) Super Junction Power MOSFET

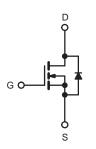
PRODUCT SUMMARY						
V <sub>DS</sub> (V)	90	900				
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V	1.3				
Q <sub>g</sub> (Max.) (nC)	200	200				
Q <sub>gs</sub> (nC)	24	24				
Q <sub>gd</sub> (nC)	110	110				
Configuration	Sing	Single				

#### **FEATURES**

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC







N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			$V_{DS}$	900	V	
Gate-Source Voltage			$V_{GS}$	± 20	V	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	5		
Continuous Drain Current	VGS at 10 V	T <sub>C</sub> = 100 °C		3.9	Α	
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	21			
Linear Derating Factor		1.5	W/°C			
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	770	mJ	
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	7.8	Α	
Repetitive Avalanche Energy <sup>a</sup>		E <sub>AR</sub>	19	mJ		
Maximum Power Dissipation $T_C = 25  ^{\circ}C$			P <sub>D</sub>	190	W	
Peak Diode Recovery dV/dt <sup>c</sup>		dV/dt	2.0	V/ns		
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	eak Temperature) for 10 s			300 <sup>d</sup>	7	
Mounting Torque	6 32 or N	M2 sorow		10	lbf ⋅ in	
Mounting rorque	6-32 or M3 screw			1.1	N⋅m	

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b.  $V_{DD} = 50$  V, starting  $T_{J} = 25$  °C, L = 23 mH,  $R_{g} = 25$   $\Omega$ ,  $I_{AS} = 7.8$  A (see fig. 12). c.  $I_{SD} \le 7.8$  A, dl/dt  $\le 140$  A/ $\mu$ s,  $V_{DD} \le 600$  V,  $T_{J} \le 150$  °C. d. 1.6 mm from case.

<sup>\*</sup> Pb containing terminations are not RoHS compliant, exemptions may apply



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	40		
Case-to-Sink, Flat, Greased Surface	R <sub>thCS</sub>	0.24	-	°C/W	
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	0.65		

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static						,	
Drain-Source Breakdown Voltage	$V_{DS}$	V <sub>GS</sub>	= 0 V, I <sub>D</sub> = 250 μA	900	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C, I <sub>D</sub> = 1 mA	-	0.98	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> :	= V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.0	٧
Gate-Source Leakage	I <sub>GSS</sub>		V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zava Cata Valtaga Dvain Cuwant	I <sub>DSS</sub>	V <sub>DS</sub> :	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 0 V		-	100	
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 640 \	/, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	500	μA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	$I_D = 3.7 \text{ A}^b$	-	1.3	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =	: 100 V, I <sub>D</sub> = 3.7 A <sup>b</sup>	5.6	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V,		-	3100	-	pF
Output Capacitance	C <sub>oss</sub>	1	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$		800	-	
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1.0 MHz, see fig. 5		-	490	-	
Total Gate Charge	$Q_g$			-	-	200	nC
Gate-Source Charge	$Q_{gs}$	V <sub>GS</sub> = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 3.8 \text{ A}, V_{DS} = 400 \text{ V},$ see fig. 6 and 13 <sup>b</sup>		-	24	
Gate-Drain Charge	$Q_{gd}$	3cc lig. o and 10		-	-	110	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400 \text{ V}, I_{D} = 3.8 \text{ A},$ $R_{g} = 6.2 \Omega, R_{D} = 52 \Omega$ see fig. $10^{b}$		-	19	-	ns
Rise Time	t <sub>r</sub>			-	38	-	
Turn-Off Delay Time	$t_{d(off)}$			-	120	-	
Fall Time	t <sub>f</sub>			-	39	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	5.0	-	ъЦ
Internal Source Inductance	L <sub>S</sub>			-	13	-	- nH
Drain-Source Body Diode Characteristic	s					•	
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5.0	
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	21	A
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 3.8 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.8	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T.=	25 °C. I₅ = 3.8 A.	-	650	980	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	$T_J = 25  ^{\circ}\text{C}, I_F = 3.8  \text{A},$ $dI/dt = 100  \text{A/µs}^b$		-	3.8	5.7	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and I			L <sub>D</sub> )		

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. Pulse width  $\leq$  300 µs; duty cycle  $\leq$  2 %.



#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

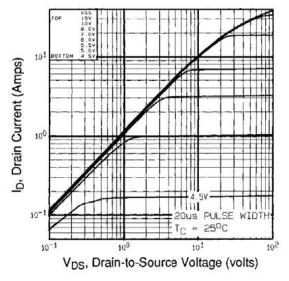


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C

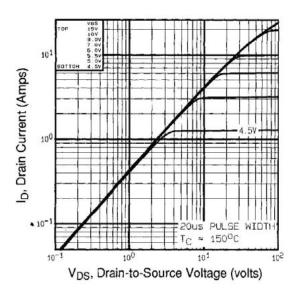


Fig. 2 - Typical Output Characteristics,  $T_C$  = 150 °C

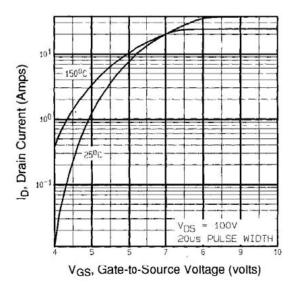


Fig. 3 - Typical Transfer Characteristics

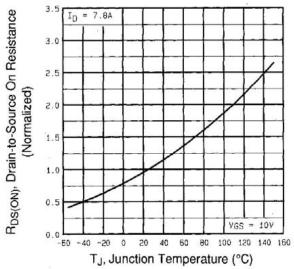


Fig. 4 - Normalized On-Resistance vs. Temperature



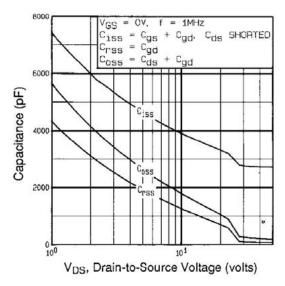


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

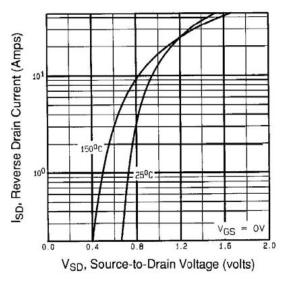


Fig. 7 - Typical Source-Drain Diode Forward Voltage

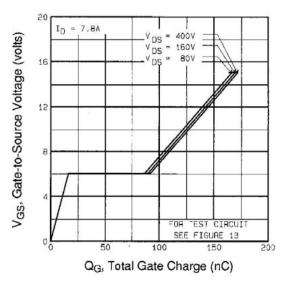


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

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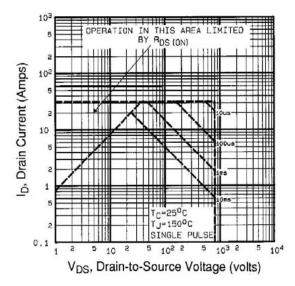


Fig. 8 - Maximum Safe Operating Area



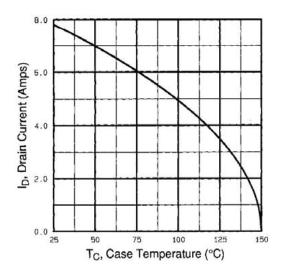


Fig. 9 - Maximum Drain Current vs. Case Temperature

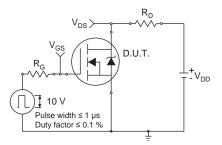


Fig. 10a - Switching Time Test Circuit

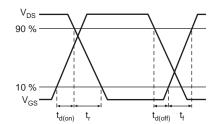


Fig. 10b - Switching Time Waveforms

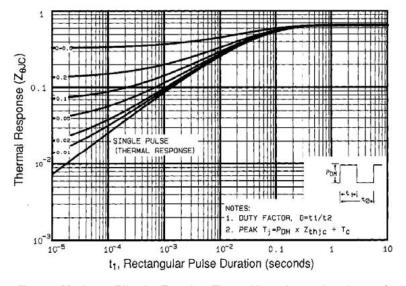


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



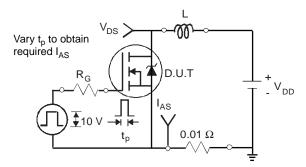


Fig. 12a - Unclamped Inductive Test Circuit

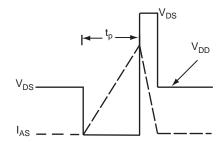


Fig. 12b - Unclamped Inductive Waveforms

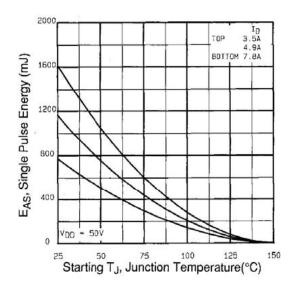


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

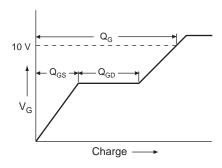


Fig. 13a - Basic Gate Charge Waveform

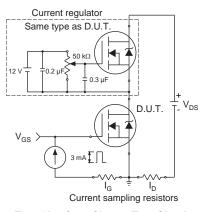
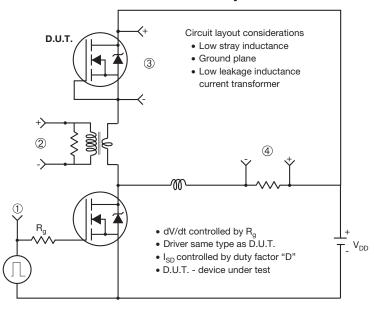


Fig. 13b - Gate Charge Test Circuit



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#### Peak Diode Recovery dV/dt Test Circuit



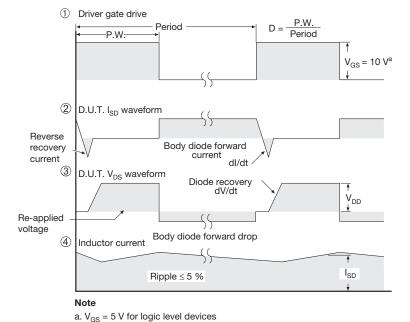
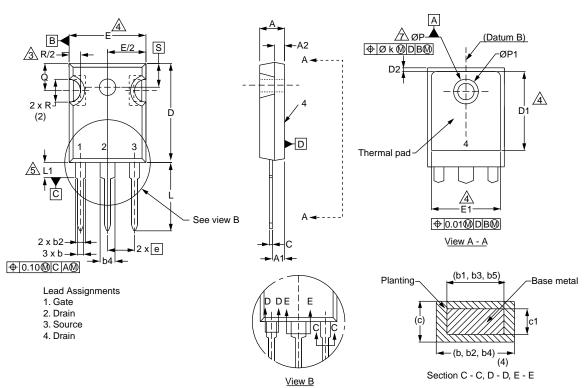


Fig. 14 - For N-Channel



# **TO-247AC (High Voltage)**



	MILLIMETERS			HES
DIM.	MIN.	MAX.	MIN.	MAX.
Α	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
С	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

	MILLIMETERS		INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
D2	0.51	1.30	0.020	0.051	
Е	15.29	15.87	0.602	0.625	
E1	13.72	ı	0.540	1	
е	5.46 BSC		0.215	BSC	
Øk	0.2	0.254		0.010	
L	14.20	16.25	0.559	0.640	
L1	3.71	4.29	0.146	0.169	
N	7.62	7.62 BSC		BSC	
ØΡ	3.51	3.66	0.138	0.144	
Ø P1	-	7.39	ı	0.291	
Q	5.31	5.69	0.209	0.224	
R	4.52	5.49	0.178	0.216	
S	5.51 BSC		0.217	BSC	



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